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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,796	01/11/2002	David Glen White	RCA89647	5621

7590 06/30/2006

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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,796	WHITE ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006 and 14 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 14, 2006 and March 03, 2006 have been fully considered but they are not persuasive.

In re pages 4-6, applicants argue, with respect to claim 1, that nowhere does Akira disclose that clock signals are generated by the processor, that nowhere does Akira disclose that clock signals of any kind are coupled to a buffer via a digital bus, and nowhere does Akira disclose that the buffer selectively coupled the clock signals of a clock input of a noise intolerant device upon receipt of control signal because Akira is totally silent as to clock signals and it cannot be inferred that such clock signals are generated by the processor, provided to the buffer, or provided from the buffer to the noise intolerant device.

In response, the examiner respectfully disagrees. It is noted that address bus 7 of Akira carries the clock signals to be decoded by the binary-decimal decoder 9. The outputs of the binary-decimal decoder control the read and write of memories 3 and 4. It is further noted that the information in the address bus 7 is generated by the CPU 2 and is inputted to the peripheral element 8. The peripheral element 8 of Akira anticipates the claimed noise intolerant device and the CPU 2 of Akira anticipates the claimed processor. The CPU 2 of Akira generates the clock signals, which are coupled to a buffer (memories 3 and 4 of Akira) via a digital bus (address bus 7 of Akira). The memories 3 and 4 of Akira selectively coupled the clock signals (information in the address bus 7 of Akira) of a clock input of a noise intolerant device (the peripheral

element 8 of Akira) upon receipt f control signal (the outputs of the binary-decimal decoder 9 of Akira). Thus, Akira does indeed disclose all the claimed limitations.

In re pages 6-7, applicants argue, with respect to claim 2, that there is no teaching or suggestion in either Akira or Tults to provide the IIC bus and IIC bus expander into Akira because the IIC bus system is a particular bus system that utilizes particular IIC components.

In response, the examiner respectfully disagrees. The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

Finally, the expected benefits from IIC bus disclosed in col. 1, lines 12-30 of Tults et al would themselves have been evidence of obviousness. Expected beneficial results are themselves evidence of obviousness. In re Hoffman, 556 F.2d 539, 194 USPQ 126 (CCPA 1977); In re Skoll, 523 F.2d 1392, 187 USPQ 481 (CCPA 1975); and In re Skoner, 517 F.2d 947, 186 USPQ 80 (CCPA 1975).

In re page 7, applicants argue, with respect to claim 3, that claim 3 is not obvious over Akira and Tults for the same reasons as discussed in claim 1 above.

In response, as discussed in claim 1 above, Akira discloses all the claimed limitations of claim 1.

In re pages 7-8, applicants argue, with respect to claim 4, that claim 4 is not obvious over Akira and Tults for the same reasons as discussed in claim 1 above.

In response, as discussed in claim 1 above, Akira discloses all the claimed limitations of claim 1.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipate by Ishida Akira (JP Publication No. 60144857 A).

In considering claim 1, Ishida Akira discloses all the claimed subject matter, note 1) the claimed a processor for producing clock and data signals and a control signal is met by the CPU 2 (Fig. 2, page 3, lines 15-29), 2) the claimed a digital bus that couples said clock and data signals to a buffer is met by the data bus 5 or 6 (Fig. 2, page 3, lines 15-29), 3) the claimed where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device is met by the bus buffer 1 which separates or connects the data bus 6 (connected to peripheral element 8) from or to data bus 5 (Fig. 2, page 3, lines 15-29).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida Akira (JP Publication No. 60144857 A) in view of Tults et al (US Patent No. 6,693,678 B1).

In considering claim 2, Ishida Akira discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein said digital bus is an inter integrated circuit (IIC) bus, and the apparatus further comprises an IIC bus expander for transferring said control signal to said buffer. Tults et al teach that in a conventional data bus system such as the IIC bus system shown in Fig. 1, master device 2 is connected to slave device 4 (designed slave #1 by IIC bus 6 (Figs. 1 and 3, col. 3, lines 40-62). Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the IIC bus as taught by Tults et al into Ishida Akira's system in order to transfer the data and clock signals which large loads at high speed to perform the communication between master and slave devices as fast as possible.

Additionally, the capability of using an IIC bus expander is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the old and well known

of using an IIC bus expander into Ishida Akira's system in order to expand the bandwidth of the IIC bus.

In considering claim 3, Tults discloses all the claimed subject matter, note 1) the claimed wherein the digital bus comprises an IIC bus having a clock signal path for transferring clock pulses from said processor to said clock inputs of an IIC bus expander and said buffer is met by the bus line SCL (Fig. 3, col. 4, lines 41-58), 2) the claimed a data signal path for transferring data from said processor on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander and said buffer is met by the bus line SDA (Fig. 3, col. 4, lines 41-58), and 3) the claimed wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device from said IIC bus and said processor is met by the tri-state buffers 15 and 16 (Fig. 3, col. 4, line 59 to col. 6, line 4).

In considering claim 4, the claimed wherein said noise intolerant device comprises: a tuner, coupled to said clock and data outputs of said buffer device, having a phase-lock loop for generating frequency variable tones, and a down-converter coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal is met by the tuner of the television receiver (col. 1, line 11 to col. 2, line 28 of Tult et al).

Allowable Subject Matter

6. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TT
June 22, 2006

Trang U. Tran
Examiner
Art Unit 2622